IFW 2811 AR

Docket No.: 50090-290

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Keiichiro WAKAMIYA, et al.	:	Confirmation Number: 2402
Serial No.: 09/818,906	:	Group Art Unit: 2811
Filed: March 28, 2001	:	Examiner: Nitin Parekh
For: SEMICONDUCTOR DEVICE	:	

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed May 25, 2004. Please charge the Appeal Brief fee of 330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed May 25, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is Renesas Technology Corp.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related Appeal or Interference.

III. STATUS OF CLAIMS

Claims 1 through 13 are pending in this Application and have been finally rejected. It is from the final rejection of claims 1 through 13 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the issuance of the Final Office Action dated March 9, 2004.

V. SUMMARY OF INVENTION

The present invention is directed to a semiconductor device comprising a semiconductor chip and a protective insulating layer covering the surface of the semiconductor chip (page 2 of the written description of the specification, lines 16 through 18). A conventional chip-scale package (CSP) with solder balls functioning as external terminals subsequent to resin encapsulation is schematically illustrated in Fig. 3 (page 1 of the written description of the specification, lines 17 through 24). Adverting to Fig. 3, reference character 4 designates a connecting conductor or post; reference character 6 denotes a bump as an external terminal; and reference character 7 designates a coating layer (paragraph bridging pages 1 and 2 of the written description of the specification). Such devices are problematic because of a difference in coefficients of linear expansion between the semiconductor chip 1 and the sealing resin 5, which imposes a stress on posts 4 resulting in cracking (page 2 of the written description of the specification, second full paragraph). The present invention addresses and solves that problem by forming the connecting conductor as a plurality of layers, at least one of which is a stress-absorbing layer having a lower hardness than the other layer (page 2 of the written description of

the specification, lines 22 through 25). The layers of the connecting conductor can be made of the same materials (independent claim 1) or different materials (independent claim 7).

The notion of providing a stress absorbing layer as a layer in a connecting conductor penetrating beyond the outer surface of the coating layer and connected to an external bump terminal is alien to the applied prior art.

VI. ISSUES

A. The Rejections:

1. Claim 1 was rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al;

2. Claims 2 and 3 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Akagawa;

3. Claims 4 through 6 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Khoury;

4. Claims 7 and 8 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Chakravorty;

5. Claims 9 and 10 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Akagawa; and

6. Claims 11 through 13 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Khoury.

B. The Issues Which Arise in This Appeal and Require Resolution by the Honorable Board of Patent Appeals and Interferences (the Board) Are:

1. Whether claim 1 is unpatentable under 35 U.S.C. § 103 for obviousness predicated Yamaji et al. in view of Ohtsuka et al.;

2. Whether claims 2 and 3 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Akagawa;

3. Whether claims 4 through 6 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Khoury;

4. Whether claims 7 and 8 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Chakravorty;

5. Whether claims 9 and 10 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Akagawa; and

6. Whether claims 11 through 13 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Khoury.

VII. GROUPING OF CLAIMS

The appealed claims do **not** stand or fall together as a group. Claims 1 through 6 stand or fall together with independent claim 1. Claims 7 through 13 stand or fall together with independent claim 7.

VIII. THE ARGUMENT

1. **The Rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al.**

The Examiner's Position

In the statement of the rejection the Examiner made certain inaccurate factual determinations as to the teachings of Yamaji et al., committed legal error in announcing the motivational element, eschewed an indicium of nonobviousness and then committed legal error in the ultimate conclusion of obviousness under 35 U.S.C. § 103.

Specifically, the Examiner referred to Fig. 3 of Yamaji et al. asserting the disclosure of a semiconductor device perceived to contain features inaccurately said to be similar to those of the claimed invention, and admitted that:

> "Yamaji et al. fail to teach at least one of the connecting conductor layer being formed as a stress absorbing layer having lower hardness than the other layer" (page 3 of the March 9, 2004 Final Office Action, lines 9 and 10).

This admitted shortcoming of Yamaji et al. is no small matter, but represents one of the major differences between the claimed invention and the semiconductor device disclosed by Yamaji et al. The Examiner then resurrected Ohtsuka et al., a reference previously applied but then discarded, and concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device disclosed by Yamaji et al. by providing a stress absorbing layer. The factual basis for that conclusion remains a mystery, since the Examiner **failed to identify** wherein either of the applied references suggests the notion of employing a stress absorbing layer.

Appellants' Position

The Examiner's determination as to the teachings of the applied references are factually inaccurate. Specifically, according to independent claim 1, the connecting conductors, which are not part of a wiring layer, penetrate the coating layer 7 (Fig. 1). In the semiconductor device disclosed by Yamaji et al., the Examiner identified as a protective coating layer element 5 in Fig. 3, and connecting conductors 4a and 6. But connecting conductor 4a of Yamaji et al. does not, however, correspond to a connecting conductor of the claimed invention, because it is a **wiring layer** which is specifically precluded from being a connecting conductor by express language in claim 1. Yamaji et al. refer to barrier metal layer 4 as "a lead pattern 4 of barrier metal" (column 5 of Yamaji et al., lines 55 and 56). What Yamaji et al. define as a "lead pattern", the Examiner converts to a connecting conductor committing legal error by ignoring the express claim language of claim 1 **precluding** the connecting conductor from being part of a wiring layer. Therefore, the only thing Yamaji et al. disclose is a wiring layer penetrating a coating layer. Yamaji et al. neither disclose nor suggest the notion of providing a connecting conductor, which is not part of a wiring layer, penetrating the coating layer.

Ohtsuka et al. do not help the Examiner's cause, because Ohtsuka et al. merely disclose diffusion barriers which also correspond to wiring layers. Moreover, these diffusion barrier layers are between electrode pads and external terminals and are formed within the protective insulating layer 34. Therefore, the reference to Ohtsuka et al. merely discloses a plurality of barrier layers between electrode pads and external terminals. Ohtsuka et al. **do not** disclose any connecting member that is not part of a wiring layer and **protrudes** from the protective insulating film 34.

In order to establish the requisite realistic motivation, the Examiner must clear and particular make factual determinations and, based upon such factual determinations, provide reasons **why** one having ordinary skill in the art would have been realistically impelled to **restructure** the device disclosed by Yamaji et al. by forming a plurality of connecting conductors wherein one of the conductive layers is a stress absorbing layer of lower hardness. *Teleflex Inc. v. Ficosa North America Corp., 299 F.3d 1313, 63 USPQ2d 1374; In re Lee, 237 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).* That the Examiner did not comply with this judicial mandate is understandable, because it is no easy task, particularly since the Examiner cannot even identify wherein the device disclosed by Yamaji et al. has any connecting conductors not part of a wiring layer penetrating the coating layer as claimed. The Examiner merely points to **diffusion barrier layers formed within the protective insulating layer 34** of the device disclosed by Ohtsuka et al. in Fig. 3, and then announces the obviousness conclusion. This approach is **legally erroneous**. *In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); Grain Processing Corp. v. American-Maize Products Co., 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).*

The Examiner's error is exacerbated by the fact that the Examiner failed to point out wherein Ohtsuka et al., the allegedly teaching reference, actually provides any teaching to form a stress absorbing layer. Ohtsuka et al. only care about diffusion barriers.

It is **not** apparent and the Examiner did **not provide a fact-based explanation why** one having ordinary skill in the art would have realistically zeroed in on the diffusion barrier layers (part of a wiring layer) formed **within** protective layer 34 in the device disclosed by Ohtsuka et al. in Fig. 3 for any reason to modify the device disclosed by Yamaji et al. in Fig. 3, apart from **improper reliance upon Applicants' disclosure**. *Panduit Corp. v. Dennison Mfg. Co., 774 F.2d 1082, 227 USPQ 337*

(Fed. Cir. 1985). There is conspicuously missing from the Examiner's case the idea of providing a stress absorbing layer. Appellants stress that concept is found **only** in Appellants' disclosure. *Panduit Corp. v. Dennison Mfg. Co., supra.*

To whatever extent the Examiner's rejection is predicated upon the theory that **if**, and that is a big **if** with which Appellants do not agree, one having ordinary skill in the art would have somehow decided to replace the specifically structured conductive **barrier metal** 4a in the Fig. 3 device of Yamaji et al. with the unrelated diffusion barrier 35 of the Fig. 3 device of Ohtsuka et al., which does **not** protrude from protective layer 34, and **if**, another big **if**, the proper combination of diffusion layers is **fortuitously** selected, **then**, perhaps the claimed invention would result, such an approach has been repeatedly judicially condemned as confusing obviousness with inherency and, hence, legally erroneous. *In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); In re Shetty, 566 F.2d 81, 195 USPQ 753 (CCPA 1977); In re Naylor, 369 F.2d 765, 152 USPQ 106 (CCPA 1966); In re Henderson, 348 F.2d 550, 146 USPQ 372 (CCPA 1965).* Indeed, as articulated by the Honorable Board of Patent Appeals and Interferences in *Ex parte Schricker, 56 USPQ2d 1723, 1725:*

> Inherency and obviousness are somewhat like oil and water-they do not mix well.

It should, therefore, be apparent that the Examiner did not establish a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis and want of the requisite realistic motivation.

Evidence of Nonobviousness

The Examiner's allegedly teaching reference to Ohtsuka et al. clearly **teaches away** from forming the diffusion barrier layers (not stress absorbing layers) so that they protrude from the protection layer 34. Although the barrier diffusion layer 35/36 may be thinner than the protection layer 34, it is preferred to be identical in thickness. See, for example, column 5 of Ohtsuka et al., second and third full paragraphs. If, as the Examiner contends, Ohtsuka et al. teach one having ordinary skill in the art how to modify the device disclosed by Yamaji et al., then one having ordinary skill in the art would have formed the conductive barrier metal 4a so that it does **not** extend above or out of protective film 3 and, hence, would **not** satisfy the requirements of the claimed invention. Thus, Ohtsuka et al. **clearly teach away** from the claimed invention. Such a **teaching away** from the claimed invention by the Examiner's allegedly teaching reference constitutes **clear evidence of nonobviousness**. *In re Bell, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); Specialty Composites v. Cabot Corp., 845 F.2d 981, 6 USPQ2d 1601 (Fed. Cir. 1988); In re Hedges, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); In re Marshall, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).*

Conclusion

Based upon the foregoing, it should be apparent that a *prima facie* basis to deny patentability to the claimed invention has not been established for lack of the requisite factual basis and want of the requisite realistic motivation. Moreover, upon giving due consideration to the **clear teaching away** from the claimed invention by the Examiner's allegedly teaching reference to Ohtsuka et al., the conclusion appears inescapable that one having ordinary skill in the art would **not** have found the claimed invention **as a whole** obvious within the meaning of 35 U.S.C. §103. *In re Piasecki, 745 F.2d*

1468, 223 USPQ 785 (Fed. Cir. 1984). Applicants, therefore, submit that the imposed rejection of claim 1 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. is not factually or legally viable.

2. The rejection of claims 2 and 3 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Akagawa; and

3. The rejection of claims 4 through 6 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Khoury.

Claims 2 through 6 stand or fall with independent claim 1. Neither Akagawa nor Khoury cures the previously argued deficiencies in the attempted combination of Yamaji et al. and Khoury.

4. The rejection of claims 7 and 8 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Chakravorty.

The Examiner's Position

In the statement of the rejection, the Examiner again concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device disclosed by Yamaji et al., which admittedly does not disclose the concept of providing a stress absorbing layer, in view of Ohtsuka et al. by providing a stress absorbing layer, even though Ohtsuka et al. do not speak in terms of a stress absorbing layer. The Examiner further concluded that one having ordinary skill in the art would have been motivated to form one of the connecting conductor layers of a different material in view of Chakravorty.

A. **Appellants' Position**

As argued in addressing the patentability of claim 1, Yamaji et al. call barrier metal 4 a "lead pattern" (column 7, line 56), e.g. Hence, barrier metal 4a identified by Examiner cannot, by the terms of claim 7, be a connecting conductor because it is part of a wiring layer.

Similarly, Ohtsuka et al. merely disclose wiring layers (diffusion barriers), which cannot correspond to the connecting conductor of the claimed invention. Moreover, Ohtsuka et al. only disclose wiring layers which penetrate a coating layer, not a connecting conductor penetrating the coating layer as in the claimed invention.

Appellants stress the device disclosed by Ohtsuka et al. in Fig. 3 merely contains diffusion barriers formed entirely within, and required not to protrude from, the protective layer 34. It is not apparent and, as a factual matter, the Examiner has **not** established that one having ordinary skill in the art somehow have been realistically lured to zero in on the diffusion barriers formed **within** protective layer 34 of the device depicted by Ohtsuka et al. in Fig. 3 for any reason to modify the conductive barrier metal (wiring) layer 4a in the device depicted in Fig. 3 of Yamaji et al. *Teleflex Inc. v. Ficosa North America Corp., supra; In re Lee, supra.* As also previously argued, the Examiner confuses obviousness with inherency by attempting to combine the applied references and then arrive at the claimed invention by resorting to the doctrine of inherency. Inherency requires certainty not the fortuitous selection of elements upon combining references. *Ex parte Schricker, supra: In re Rijckaert, supra, In re Shetty,, supra; In re Naylor, supra; In re Henderson, supra.* Moreover, as also previously argued, Ohtsuka et al. **clearly teach away** from the claimed invention by requiring formation of the diffusion barriers entirely within the protective layer. This **teaching away** from the claimed invention constitutes clear evidence of **nonobviousness**. *In re Bell, supra; Specialty Composites v. Cabot Corp.,*

supra; In re Hedges, supra; In re Marshall, supra. The additional reference to Chakravorty does not cure the argued deficiencies in the attempted combination of Yamaji et al. and Ohtsuka et al.

It should, therefore, be apparent that a *prima facie* basis to deny patentability to the claimed invention has not been established for lack of the requisite factual basis in want of the requisite realistic motivation. Moreover, the **clear teaching away** from the claimed invention by Ohtsuka et al. constitutes potent evidence of **nonobviousness** which undermines the conclusion that one having ordinary skill in the art would **not** have found the claimed invention **as a whole** obvious within the meaning of 35 U.S.C. §103. *In re Piasecki, supra.* Appellants, therefore, submit that the imposed rejection of claims 7 and 8 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al. and Chakravorty is not factually or legally viable.

5. The rejection of claims 9 and 10 under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Akagawa, and

6. The rejection of claims 11 through 13 were rejected under 35 U.S.C. §103 for obviousness predicated upon Yamaji et al. in view of Ohtsuka et al., Chakravorty and Khoury.

Claims 9 through 13 stand or fall together with claim 7. The additional reference to Akagawa Khaury do not cure the above-argued shortcomings and in the attempted combination of Yamaji et al., Ohtsuka et al. and Chakravorty.

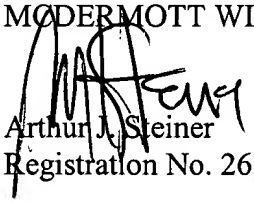
IX. PRAYER FOR RELIEF

Based upon the arguments submitted *supra*, Appellants submit that each of the Examiner's rejections under 35 U.S.C. § 103 is not factually or legally viable. Appellants, therefore, solicit the Honorable Board to reverse each of the Examiner's rejections under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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X. APPENDIX

1. A semiconductor device comprising:

a semiconductor chip,

a protective insulating layer comprising a coating layer covering the surface of the semiconductor chip;

a plurality of connecting conductors connected to the surface of the semiconductor chip and penetrating the coating layer beyond the outside surface of the coating layer, wherein the connecting conductors are connected to bumps as external terminals beyond the outside surface of the coating layer, and wherein the connecting conductors do not include wiring layers and the bumps;

wherein the connecting conductor includes a plurality of layers formed of same material and at least one of the layers is formed as a stress-absorbing layer having lower hardness than other layer.

2. The semiconductor device according to claim 1, wherein said connecting conductor is formed from anisotropic conductive material.

3. The semiconductor device according to claim 1, wherein said connecting conductor is formed from conductive material containing metal particles.

4. The semiconductor device according to claim 1, wherein said connecting conductor is formed by means of stacking a plurality of layers in a staggered manner.

5. The semiconductor device according to claim 4, wherein said plurality of layers of the connecting conductor are formed in substantially identical diameter.

6. The semiconductor device according to claim 4, wherein said plurality of layers of the connecting conductor are formed in different diameters from each other in sequence of layers.

7. A semiconductor device comprising:

a semiconductor chip,

a protective insulating layer comprising a coating layer covering the surface of the semiconductor chip;

a plurality of connecting conductors connected to the surface of the semiconductor chip and penetrating the coating layer beyond the outside surface of the coating layer, wherein the connecting conductors are connected to bumps as external terminals beyond the outside surface of the coating layer, and wherein the connecting conductors do not include wiring layers and the bumps;

wherein the connecting conductor includes a plurality of layers formed of different material and at least one of the layers is formed as a stress-absorbing layer having lower hardness than other layer.

8. The semiconductor device according to claim 7, wherein said stress-absorbing layer is formed from gold and palladium.

9. The semiconductor device according to claim 7, wherein said stress-absorbing layer is formed from anisotropic conductive material.

10. The semiconductor device according to claim 7, wherein said stress-absorbing layer is formed from conductive material containing metal particles.

11. The semiconductor device according to claim 7, wherein said connecting conductor is formed by means of stacking the plurality of layers in a staggered manner.

12. The semiconductor device according to claim 11, wherein said plurality of layers of the connecting conductor is formed in substantially identical diameter.

13. The semiconductor device according to claim 11, wherein said plurality of layers of the connecting conductor are formed in different diameters from each other in sequence of layers.